

## Claims

What is claimed is:

1. A data readout integrated circuit comprising a plurality of inputs coupled to a plurality of detectors, plurality of inputs coupled to plurality of input amplifiers, for providing a plurality of readout signals amplified from the plurality of detector signals, each input amplifier is part of a readout channel of said plurality, said readout channels comprising:
  - a means for receiving one detector signal;
  - a charge sensitive amplifier coupled to said receiving means for integrating said detector signal and outputting a voltage signal;
  - 10 a processing circuit for processing the said charge sensitive amplifier output, and
  - a means for outputting said readout signals responsive to said detector signals.
2. The data readout integrated circuit of claim 1, wherein a polarity switching circuit is included.
3. The data readout integrated circuit of claim 2, wherein said polarity switching circuit is  
15 externally controlled.
4. The data readout integrated circuit of claim 1, further comprising a gain stage coupled to said charge sensitive amplifier.
5. The data readout integrated circuit of claim 1, further comprising a shaper amplifier for providing shaped, integrated detector signals responsive to said selected signal.
- 20 6. The data readout integrated circuit of claim 5, wherein said shaped, integrated detector signal is of an approximately inverted bell shaped form.
7. The data readout integrated circuit of claim 5, wherein said shaped, integrated detector signal is of an approximate uninverted bell shaped form.
8. The data readout integrated circuit of claim 5, further comprising a peak hold circuit coupled  
25 to output of shaper amplifier, wherein peak hold circuit have output which is coupled to a first plurality of comparators.

9. The data readout integrated circuit of claim 8, wherein a first comparator of said plurality of comparators is a low level discriminator, and wherein at least one of said first comparator allows an output trigger when a peak hold circuit output is larger than a first threshold voltage.

5 10. The data readout integrated circuit of claim 9, further comprising a second comparator of said plurality of comparators wherein said second comparator is an upper level discriminator, and wherein said second comparator only issues a signal when said peak hold circuit output is larger than a second threshold voltage.

11. The data readout integrated circuit of claim 10, wherein said first comparator and said second plurality of comparator enclose at least one predetermined energy band.

10 12. The data readout integrated circuit of claim 10, further comprising a differentiator circuit coupled to at least one of said first plurality of comparators, said differentiator circuit producing a fast trigger output with low jitter.

13. The data readout integrated circuit of claim 8, wherein an output of said peak hold circuit is multiplexed to said means for outputting.

15 14. The data readout integrated circuit of claim 10, wherein an output of at least one of said comparator or said second plurality of comparator initiates a readout cycle of said data readout integrated circuit.

20 15. The data readout integrated circuit of claim 1, wherein said data outputting means outputs a readout signal for one channel of said plurality of integrated circuit channels containing a detected signal.

16. The data readout integrated circuit of claim 15, wherein said data outputting means only outputs said readout signal for said channel of said plurality of integrated circuit channels for which a trigger signal has been received.

25 17. The data readout integrated circuit of claim 15, wherein said data outputting means outputs said readout signal for said channel of said plurality of integrated circuit channels after said trigger signal has been received for any one of said plurality of integrated circuit channels.

18. The data readout integrated circuit of claim 17, wherein said trigger signal is an external trigger signal.

19. The data readout integrated circuit of claim 1, wherein said data outputting means output a readout signal for one triggered channel of said plurality of integrated circuit channels and disables all remaining channels of said plurality of integrated circuit channels, wherein a time delay between said readout signal and said disablement of said remaining channels is controlled

5 by an externally supplied signal.

20. The data readout integrated circuit of claim 1, wherein said input charge sensitive amplifier has a resistive feedback in parallel to the capacitance feedback.